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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/386,646	08/31/99	FAZAN	P 660073.488D1

MMC2/0815

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EXAMINER	
VU, H	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/15/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/386,646	GAZAN ET AL.
Examiner	**Art Unit**
HUNG VU	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 24, 2001*

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22 and 24-37* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideratio

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22 and 24-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some* c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)

16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *11*

18)☐ Interview Summary (PTO-413) Paper No(s). _____

19)☐ Notice of Informal Patent Application (PTO-152)

20)☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 34 is rejected under 35 U.S.C. 102(b) as being anticipated by Shimbo (PN 4,980,306, of record).

Shimbo discloses a microelectronic device comprising,

a microelectronic substrate (1) having a trench formed therein;

a field oxide (17) within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide;

a component (304) formed on the field oxide. Note Figures 2f and 3a of Shimbo.

2. Claims 22 and 28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima et al. (PN 5,329,482).

Nakajima et al. discloses a microelectronic device comprising,

a microelectronic substrate (1);

a gate structure including a gate oxide layer (5) formed on the substrate, a first gate layer (6) formed on the gate oxide layer, and an adhesion layer (7) formed on the first gate layer, the gate structure having a trench at least partially disposed therein and extending into the substrate;

a field oxide layer (2) at least partially in the trench having substantially straight sides not contact the gate oxide layer and extending upwardly from the trench and not extending laterally from the trench over an upper surface of the substrate, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer;

an oxide spacer (8) adjacent the gate structure. Note Figures 5-13 of Nakajima et al..

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22 and 24-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (PN 5,296,400) in view of Manning (PN 5,177,028, of record).

Park et al. discloses a microelectronic device comprising,

a microelectronic substrate (1);

a gate structure including a gate oxide layer (4) formed on the substrate, a first gate layer (lower portion of 5) formed on the gate oxide layer, and an adhesion layer (upper portion of 5) formed on the first gate layer, the gate structure having a field oxide layer (3) at least partially disposed therein and extending into the substrate;

the field oxide layer not contact the gate oxide layer, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate;

further comprising an oxide spacer (7) adjacent the component. Note Figures 1A-2H of Park et al..

Park et al. discloses the field oxide is a LOCOS. Park et al. does not disclose the field oxide is a trench isolation. However, Manning discloses a microelectronic device comprising a trench isolation (22). Note Figures 1-20 of Manning. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the field oxide of Park et al. by trench isolation, such as taught by Manning in order to prevent the bird-effect and further isolate the devices from each others.

With regard to claims 24-25, Park et al. and Manning do not disclose the structure further comprising a silicide layer formed on the adhesion layer. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a silicide layer on the adhesion layer because this structure reduces the contact resistance.

With regard to claim 35, Park et al. does not disclose the first gate layer comprise a polysilicon layer. However, Manning discloses the first gate layer (106) comprise a polysilicon layer. Note Figures 1-20 of Manning. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first gate layer of Park et al. comprises a polysilicon layer, such as taught by Manning because polysilicon is commonly and easy to form as the gate layer.

4. Claim 22, 24, 25, 28, 29, and 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (PN 4,935,802) in view of Manning (PN 5,177,028, of record). Noguchi et al. discloses a microelectronic device comprising,

a microelectronic substrate (11);

a gate structure including a gate oxide layer formed on the substrate, a first gate layer formed on the gate oxide layer, and an adhesion layer formed on the first gate layer, and a conductive layer formed on the adhesion layer;

the field oxide layer extending beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, the filed oxide layer not contact the gate oxide layer and not extending laterally over the surface of the substrate. Note Figures 1-4 of Noguchi et al..

Noguchi discloses the field oxide is a LOCOS. Noguchi et al. does not disclose the field oxide is a trench isolation. However, Manning discloses a microelectronic device comprising a trench isolation (22). Note Figures 1-20 of Manning. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the field oxide of Noguchi et al. by trench isolation, such as taught by Manning in order to prevent the bird-effect and further isolate the devices from each others.

With regard to claims 24, Noguchi et al. and Manning do not disclose the conductive layer is a silicide layer. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive layer of Noguchi et al. and Manning as a silicide layer in order to reduce the contact resistance.

With regard to claims 29, 31, and 33, Noguchi et al. and Manning do not disclose an oxide spacer adjacent the gate structure. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate structure of Noguchi et al. and Manning

having an oxide spacer because such structure is convention to form in order to protect the gate and the source/drain region from short-circuit.

Response to Arguments

5. Applicant's arguments filed 05/24/01 have been fully considered but they are not persuasive.

It is argued, at page 11 of the Remarks, that Shimbo does not disclose a microelectronics structures including a field oxide having substantially straight sides and not extending laterally from the trench over the surface of the substrate. This argument is not convincing because Shimbo clearly discloses, as shown in Figures 2f and 3a, a microelectronics structures including a field oxide (17) having substantially straight sides and not extending laterally from the trench over the surface of the substrate. Therefore applicant claim 34 does not distinguish over the Shimbo reference.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology Center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to ***Hung Vu*** whose telephone number is **(703) 308-4079**. The Examiner is in the Office generally between the hours of 7:00 AM to 5:30 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ***Tom Thomas***, can be reached on **(703) 308-2772**.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **(703) 308-0956**.

Vu

August 10, 2001

Sara Crane
Primary Examiner